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IT IS CLAIMED:

1. A non-volatile memory formed on a substrate, comprising:

an array of non-volatile memory cells including a plurality of rows of cells extending in a first direction across the substrate and being separated in a second direction by spaces therebetween, the first and second directions being orthogonal with each other, the cells individually including source/drain regions on opposite sides of at least one electron storage element in said first direction that are shared with adjacent cells of the same row,

strips of dielectric material elongated in the first direction and extending into the substrate in the spaces between the rows of cells in order to provide electrical isolation between the memory cells of adjacent rows including isolation of their source/drain regions in said second direction,

first electrically conductive strips elongated in the second direction and spaced apart in the first direction coincident with a plurality of adjacent source/drain diffusions, the first conductive strips individually extending across and contacting source/drain regions of a plurality of adjacent rows of cells and the dielectric material strips therebetween, and

second electrically conductive strips positioned above the substrate and individually including gates therealong that are elements of adjacent memory cells.

2. The memory of claim 1, wherein the memory cells individually include a single electron storage element positioned between adjacent ones of the source/drain regions.

3. The memory of claim 2, wherein the second electrically conductive strips are elongated in the second direction and positioned in the first direction between the first electrically conductive strips.

4. The memory of claim 1, wherein the memory cells individually include at least two electron storage elements positioned between adjacent ones of the source/drain regions, the second electrically conductive strips being elongated in the first direction with their said gates positioned in spaces between electron storage elements and in between adjacent ones of the first conductive strips in said first direction.

5. The memory of any one of claims 1, 2 or 4, wherein the strips of dielectric material have been deposited in trenches formed in the substrate between adjacent rows of memory cells.

6. The memory of any one of claims 1, 2 or 4, wherein the gates of the second electrically conductive strips are erase gates individually positioned to have a charge removal coupling with a memory cell electron storage element.

7. The memory of any one of claims 1, 2 or 4, wherein memory cells individually include a select transistor between the electron storage element and one of its source/drain regions, and further wherein the gates of the second electrically conductive strips individually form gates of the select transistors.

8. The memory of any one of claims 1, 2 or 4, wherein the first electrically conductive strips are formed of doped polycrystalline silicon.

9. The memory of any one of claims 1, 2 or 4, wherein the electron storage elements are floating gates.

10. An array of rows and columns of non-volatile memory cells that individually include at least two floating gates positioned along a row with a select transistor between them and a source and a drain on opposite sides of the at least two floating gates, wherein the sources and drains of the memory cells are interconnected by doped polycrystalline silicon lines extending in a direction along columns, and word lines extending along rows above the polycrystalline silicon lines are connected to gates of the select transistors.

11. The array of claim 10, wherein the gates of the select transistors are also coupled with floating gates in a manner to erase electrons therefrom.

12. The array of claim 10, wherein the rows of memory cells are electrically isolated from one another by trenches between them that are filled with a dielectric material.

13. An array formed on a substrate of rows and columns of non-volatile memory cells that individually include at least two floating gates positioned along a row with a select transistor between them and source and drain regions on opposite sides of the at least two floating gates that are shared with adjacent cells along the row, wherein the rows are electrically isolated from one another along the substrate in a column direction by dielectric between the rows, wherein the source and drain regions are interconnected by conductive lines with lengths oriented in the column direction to contact the source and drain regions and isolation dielectric between them, and word lines extending along rows of cells that have select transistor gates therealong.

14. The array of claim 13, wherein the rows of memory cells are electrically isolated from one another by trenches between them into the substrate that are filled with a dielectric material.

15. The array of claim 13, wherein the word lines are positioned above the source and drain region interconnecting lines.

16. An array of non-volatile memory cells on a semiconductor substrate, comprising:

a two-dimensional array of floating gates arranged in rows extending in a first direction across the substrate with spaces therebetween in a second direction and columns extending in the second direction across the substrate with spaces therebetween in the first direction, said first and second directions being orthogonal with each other, a first set of spaces separating the columns of floating gates including ones of every other space across the substrate in the first direction and a second set of spaces separating the columns of floating gates including remaining ones of every other space across the substrate in the first direction and in between the first set of spaces,

source and drain diffusions spaced apart in the first direction across the substrate along the rows and coincident with the first set of spaces between columns of floating gates,

elongated electrically conductive bit lines having lengths extending across the substrate in the second direction within the first set of spaces between columns of floating gates, said bit lines individually extending over and electrically contacting a plurality of said diffusions in adjacent rows,

elongated steering gates having lengths extending across the substrate in the second direction and being spaced apart in the first direction to overlay columns of floating gates with said second set of spaces positioned between adjacent steering gates, and

elongated select gates having lengths extending across the substrate in the first direction and spaced apart in the second direction to overlay rows of floating gates, said select gates extending into said second set of spaces with capacitive coupling with floating gates adjacent the second set of spaces.

17. The memory cell array of claim 16, wherein the source and drain diffusions are electrically isolated from one another in the second direction by strips of dielectric elongated in the first direction and spaced apart in the second direction to be positioned between the rows of floating gates.

18. The memory cell array of claim 17, wherein the strips of dielectric include trenches in the substrate that are elongated in the first direction and spaced apart in the second direction to be positioned between the rows of floating gate, and a dielectric deposited in said trenches.

19. The memory of any one of claims 16-19, wherein the first electrically conductive strips are formed of doped polycrystalline silicon.

20. A method of forming an array of floating gate memory cells on a substrate from a plurality of parallel elongated strips of gate material positioned along rows of cells, comprising:

separating the strips into segments of a given length with a first set of spaces therebetween,

implanting ions into regions of the substrate through said first set of spaces in a manner that said regions are isolated from each other along and between the rows,

forming conductive lines in the first set of spaces that individually electrically contact a plurality of said substrate regions in a plurality of rows,

separating the strip segments into sub-segments having a second set of spaces therebetween, and

forming control gates along the rows over said sub-segments and conductive lines, and which extend into the second set of spaces adjacent to edges of said sub-segments with tunnel dielectric therebetween.

21. The method of claim 20 which additionally comprises forming trenches in the substrate between the strips of gate material and filling the trench with a dielectric material.

22. The method of either of claims 20 or 21, wherein the conductive lines are formed of doped polycrystalline silicon material.

23. A method of constructing an array of non-volatile memory cells on a substrate, comprising:

forming a plurality of trenches in the substrate that are elongated in a first direction across the substrate and spaced apart in a second direction across the substrate, the first and second directions being orthogonal to each other,

filling said plurality of trenches with a dielectric material,

forming a first layer of gate material in strips having lengths extending in the first direction and spaced apart in the second direction to lie between the dielectric filled trenches,

forming over the first layer of gate material a second layer of gate material in strips having lengths extending in the second direction and being spaced apart in the first direction,

covering with a first mask a first set of spaces between the second gate material layer strips including every other space across the substrate in the first direction and leaving exposed a second set of spaces between the second gate material layer strips including remaining every other space across the substrate in the first direction and in between the first set of spaces,

etching the first gate material layer strips through the exposed second set of spaces,

implanting ions into the substrate through the exposed second set of spaces, thereby to form source and drain regions in the substrate,

thereafter forming conductive strips within the exposed second set of spaces that are elongated in the second direction and individually electrically contact a plurality of the source and drain regions along their lengths,

removing the first mask to expose the first set of spaces,

etching the first gate material layer strips through the exposed first set of spaces, thereby exposing edges of the first layer strips,

forming layers of tunnel dielectric on the exposed first layer strip edges, and

thereafter forming from a third layer of gate material control gates having lengths extending in the first direction over the first and second gate material layers with the conductive strips extending into the first set of spaces in contact with the tunnel dielectric, thereby to serve as erase gates.